



iTM2011

IEEE 802.11b/g/n 1T1R WLAN + BLE 5.0 Ultra-Low Power Module Datasheet

(Preliminary)

V0.2

Revision History

Date	Revision Content	Revised By	Version
2021/09/02	- Preliminary released	Jim Leng	0.1
2021/10/08	- Update reference design	Issac Chen	0.2
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1. General Description

The iotTech iTM2011 is a highly integrated wireless module with 2.4GHz band 1T1R 11b/g/n Wi-Fi, Bluetooth Low Energy 5.0, and MCU. A single chip MCU SoC targets for applications requiring optimal RF performance, strong security, low power consumption, and small form-factor with minimal external components. Equipped with a proven SDK, iTM2011 provides customers a fast time to market solution by leveraging existing software eco system, and still keep possibilities for product differentiation.

iTM2011 features an application processor subsystem based on Andes D10F 32-bit RISC floating point core which runs at 320MHz. It includes 384KB embedded SRAM, which is peripheral addressable. Dedicated 16KB instruction cache and 16KB data cache provides great performance for the execute-in-Place (XIP) in NOR Flash.

iTM2011 has a built-in hardware crypto engine, a True Random Number Generator (TRNG), and a 2304b e-fuse block for storing chip-specific information. This combining with high efficiency security middleware library, including secure boot and Wi-Fi WPA3, the iTM2011 builds strong secure system products for smart home applications.

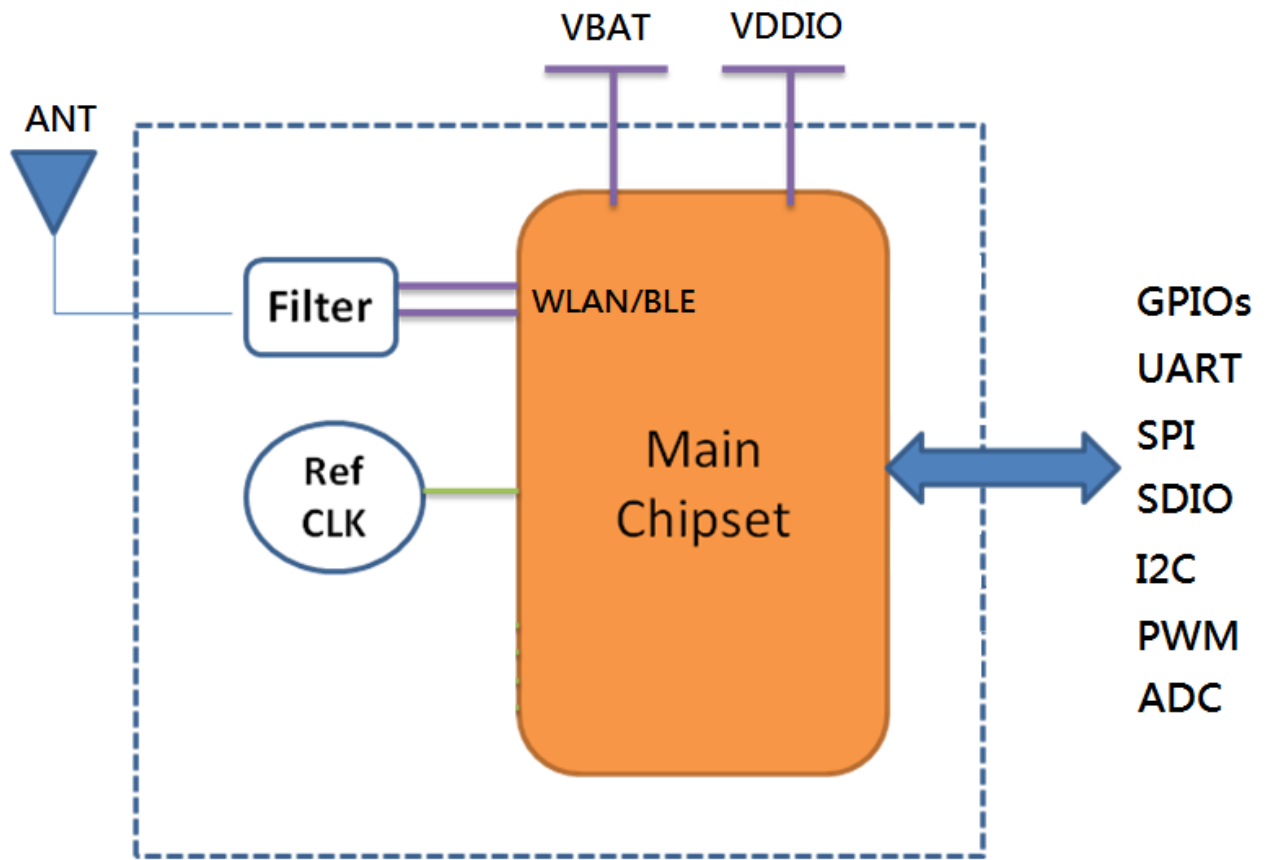
iTM2011 integrates the Balun, T/R switch, LNA, PA with advanced architecture enhancement to achieve great receive sensitivity even in noisy home scenarios. Besides, iTM2011 has very low power consumption: average 210uA at DTIM3; 33mA for receiving, and 212mA for transmission.

2. Features

- Main Chipset : iComm SV32WB01L
- System
 - Andes Technology D10F processor w/ ILM/DLM and I-cache/D-cache
 - DSP instruction set with SIMD
 - Tightly coupled single precision floating point unit (FPU)
 - Dedicated 16KB I-cache/D-cache supported
 - Memory Protection Unit (MPU) supported
 - 128KB ROM and up to 512KB SRAM for Instruction and data SRAM in total
 - Low power Dormant mode with 16KB retention SRAM
 - Low power Shut-Down mode
 - Integrated on-chip Power Management Unit (PMU) support 3.3~5V wide range
 - Security and encryption
 - AES/SHA/ECC hardware acceleration
 - Integrated True Random Number Generator
 - Integrated 2304b e-fuse and Secure boot
 - Integrate flash up to 16Mb in the package
 - Suspend/Wake-up manger controller
 - 2 DMA, each with 8 channels
 - Flash controller supports eXecute-in-Place (XIP)
 - I2C Master/Slave
 - 12-bit ADC for IOT
 - Eight PWMs
 - Four millisecond timers
 - Four microsecond timers
 - Two watchdog timers
 - All pins can be multiplexed to GPIO by user scenario
 - I2S
 - PDM Tx/Rx
- WIFI Features:
 - IEEE 802.11 b/g/n 1T1R
 - IEEE 802.11 d/e/i/k/r/w supported
 - Support 20/40MHz up to MCS7 150Mbps
 - 802.11n features supported
 - A-MPDU Tx & Rx for high MAC throughput
 - Support immediate Block-Ack
 - STA, SoftAP and Sniffer modes supported

- Concurrent STA + AP supported
- Ad-hoc, peer-to-peer and Wi-Fi Direct modes supported
- Low power Tx/Rx for short range scenario
- Low power beacon listen mode
- Low power dormant mode
- WFA features
 - WEP/WPA/WPA2/WPA3
 - WMM
- Short Guard Interval for 802.11n optimal performance
- Greenfield mode for 802.11n optimal performance
- STBC in RX mode
- Enhanced and robust sensitivity for wider coverage range
- BLUETOOTH Features
 - Bluetooth 5.0 Low Energy
 - Integrated Balun and PA
 - High power mode: up to 10 dBm
 - Rx sensitivity: -94 dBm
 - Channel assessment for AFH
 - Internal co-existence scheme between Wi-Fi and Bluetooth
 - Concurrently slave/advertiser/scanner operations supported
 - Master mode supported
 - SIG Mesh v1.01 supported
 - GATT and Mesh profile
 - Data channel long packet supported
 - Device Provision Protocol (DPP) with BLE 5.0 Extended Advertising supported
- HOST interfaces
 - High Speed UART
 - Support RX/TX/RTSN/CTSN, 4 pins
 - Baud rate up to 4.8 Mbps
 - UART
 - Support RX/TX, 2 pins
 - Baud rate up to 921,600 bps
 - SDIO 2.0
 - 1bit/4bits mode supported
 - Support Clock up to 50MHz
 - Data SPI Slave
 - Need a GPIO as RX interrupt

The block diagram of iTM2011 module is depicted in the figure below.



3. General Specification

Operating temperature	-20°C to 70°C
Storage temperature	-40°C to 85°C

3.1 Voltages

3.1.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.3	3.6	V
VDDIO	Digital IO/ SDIO Voltage	-0.3	3.6	V

3.1.2 Recommended Operating Ratings

Test conditions: At room temperature				
Symbol	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.6	V
VDDIO	1.75	3.3	3.6	V

Note: The voltage of VDDIO is depended on system I/O voltage.

Test conditions: At operating temperature -20°C ~70°C				
Symbol	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.6	V
VDDIO	1.75	3.3	3.6	V

3.2 Wi-Fi RF Specification (RX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2412		2484	MHz
RX Sensitivity 11b @ 8% PER	- 1Mbps		-95		dBm
	- 2Mbps		-93		dBm
	- 5.5Mbps		-91		dBm
	- 11Mbps		-88		dBm
RX Sensitivity 11g @ 10% PER	- 6Mbps		-91		dBm
	- 9Mbps		-90		dBm
	- 12Mbps		-88		dBm
	- 18Mbps		-86		dBm
	- 24Mbps		-82		dBm
	- 36Mbps		-79		dBm
	- 48Mbps		-74		dBm
	- 54Mbps		-73		dBm
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0		-91		dBm
	- MCS=1		-88		dBm
	- MCS=2		-86		dBm
	- MCS=3		-81		dBm
	- MCS=4		-79		dBm
	- MCS=5		-74		dBm
	- MCS=6		-73		dBm
	- MCS=7		-72		dBm
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0		-89		dBm
	- MCS=1		-85		dBm
	- MCS=2		-83		dBm
	- MCS=3		-78		dBm
	- MCS=4		-76		dBm
	- MCS=5		-71		dBm
	- MCS=6		-70		dBm
	- MCS=7		-69		dBm
Maximum Receive Level	- 802.11b		-10		dBm
	- 802.11g		-8		dBm
	- 802.11n		-8		dBm

3.3 Wi-Fi RF Specification (TX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2412		2484	MHz
Output Power	802.11b		18.0		dBm
	802.11g		14.0		dBm
	802.11n		14.0		dBm
@EVM	802.11b		-30	-10	dB
	802.11g		-30	-25	dB
	802.11n		-30	-28	dB

3.4 BLE RF Specification (RX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
RX Sensitivity			-91		dBm
Maximum Input Level		-	-	-	dBm

3.5 BLE RF Specification (TX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
Maximum Output Power		-2	5	8	dBm
20dB Bandwidth		-	-	-	MHz

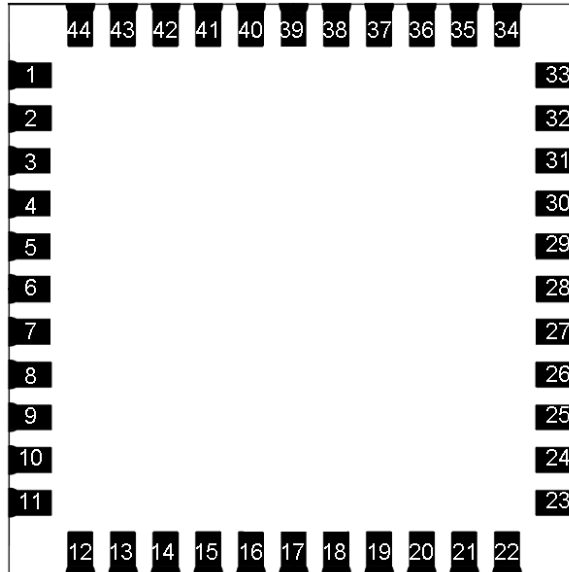
3.6 Power Consumption

WLAN Operational Modes	Typ. ^c	Unit
OFF ^a	1.5	uA
Rx, CCK, 1 Mbps ^e	33	mA
Rx, OFDM, 54 Mbps ^e	33	mA
Rx, HT20, MCS7 ^e	33	mA
Rx, HT40, MCS7 ^e	33	mA
Tx, CCK, 1 Mbps@19dBm ^d	212	mA
Tx, OFDM, 54 Mbps@15dBm ^d	182	mA
Tx, HT20, MCS7@15dBm ^d	183	mA
Tx, HT40, MCS7@15dBm ^d	183	mA
Power-saving(MCU_off) ^b , DTIM1	0.43	mA
Power-saving(MCU_off) ^b , DTIM3	0.21	mA
Power-saving(MCU_off) ^b , DTIM3 with SV32WB0xL	0.150	mA

4. Pin Assignments

4.1 PCB Pin Outline (12X12mm)

< TOP VIEW >



4.2 Pin Definition

NO	Name	Type	Description
1	GND	G	Ground connections
2	RF_OUT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Should not be connected
5	NC	—	Should not be connected
6	GPIO33	I/O	Multi-function IO33 (UART1_TX)
7	GPIO37	I/O	Multi-function IO37 (I2C_SDA / ADC7)
8	NC	—	Should not be connected
9	VBAT	P	Main power voltage source input
10	NC	—	Floating (Don't connected to ground)
11	NC	—	Floating (Don't connected to ground)
12	LDO_EN	I	WLAN device power enable/disable

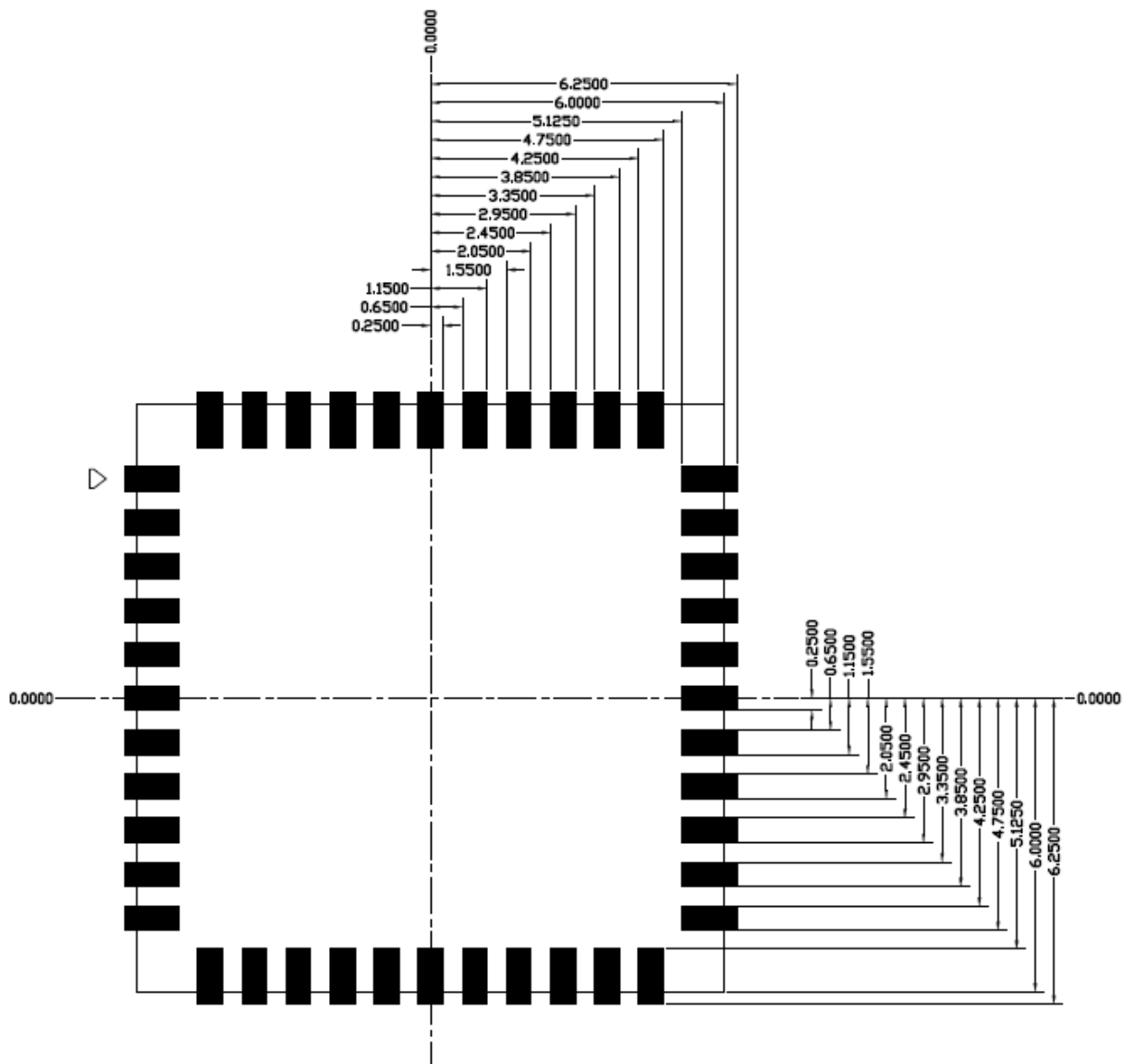
13	GPIO14	I/O	Multi-function IO14
14	GPIO17	I/O	Multi-function IO17 (SDIO DATA2)
15	GPIO18	I/O	Multi-function IO18 (SDIO DATA3 / DSPI_CSN)
16	GPIO19	I/O	Multi-function IO19 (SDIO CMD / DSPI_MOSI)
17	GPIO20	I/O	Multi-function IO20 (SDIO CLK / DSPI_CLK)
18	GPIO21	I/O	Multi-function IO21 (SDIO DATA0 / DSPI_MISO)
19	GPIO22	I/O	Multi-function IO22 (SDIO DATA1)
20	GND	G	Ground connections
21	NC	—	Should not be connected
22	VDDIO	P	I/O Voltage supply input
23	NC	—	Should not be connected
24	NC	—	Should not be connected
25	NC	—	Should not be connected
26	NC	—	Should not be connected
27	NC	—	Should not be connected
28	NC	—	Should not be connected
29	NC	—	Should not be connected
30	NC	—	Should not be connected
31	GND	G	Ground connections
32	NC	—	Should not be connected
33	GND	G	Ground connections
34	GPIO13	I/O	Multi-function IO13 / Boot Strapping Pin: 0: Normal operation; 1: Download F/W
35	NC	—	Should not be connected
36	GND	G	Ground connections
37	GPIO01	I/O	Multi-function IO01 (UART0 TX / ADC1)
38	GPIO00	I/O	Multi-function IO00 (UART0 RX / ADC0)
39	GPIO36	—	Multi-function IO36 (I2C_SCL / ADC6)
40	GPIO29	—	Multi-function IO29 (UART1_RX / ADC3)
41	NC	—	Should not be connected
42	NC	—	Should not be connected
43	NC	—	Should not be connected
44	NC	—	Should not be connected

5. Dimensions

5.1 Layout Recommendation

(Unit: mm)

< TOP VIEW >



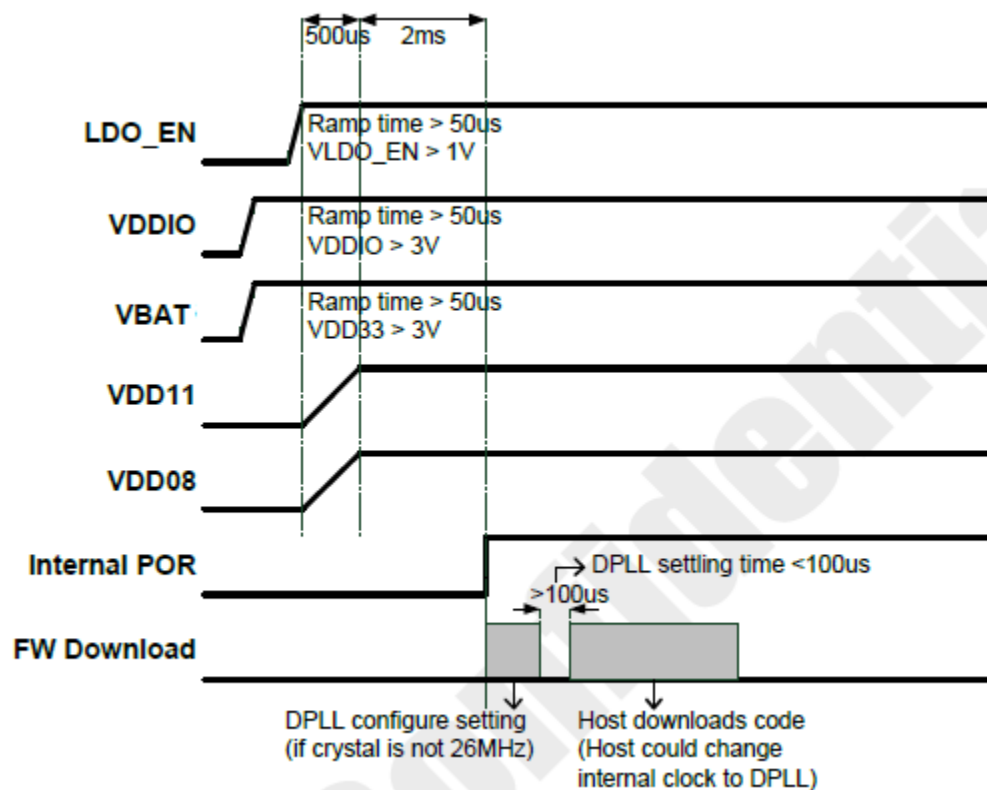
6. Host Interface Timing Diagram

6.1 Power UP Sequence

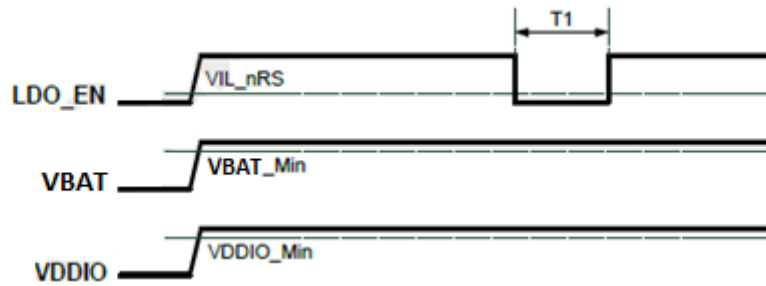
Figure below shows the $VDD33=3.3V$ power-on sequence of the iTM2011 from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept above the threshold voltage. After initial power-on, the LDO_EN signal can be held low to turn off the iTM2011 or pulsed low to induce a subsequent reset.

After LDO_EN is asserted, the host starts the power-on sequence of the iTM2011. From that point, the typical iTM2011 power-on sequence is shown below:

1. Within $T1+2.5ms$, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.



6.2 Reset Timing



Parameters	Description	Min.	Unit
T1	Duration of LDO_EN signal level < VIL_nRST(refer to its value in Table 9: Recommended Operating Conditions and DC Characteristics) to reset the chip	500	us

6.3 SDIO Characteristics

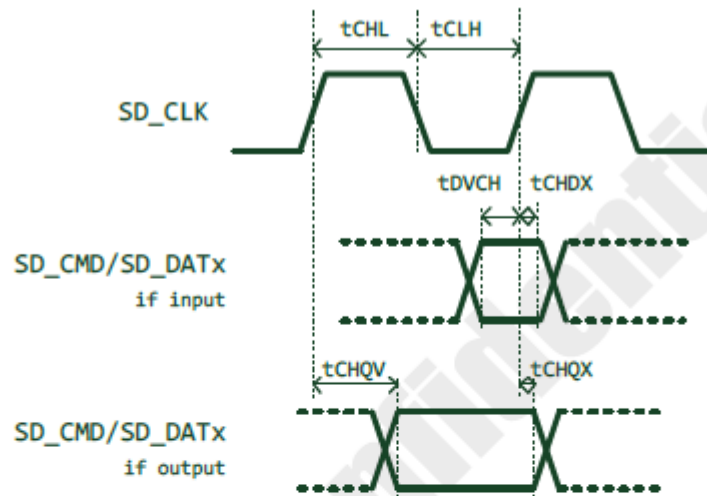
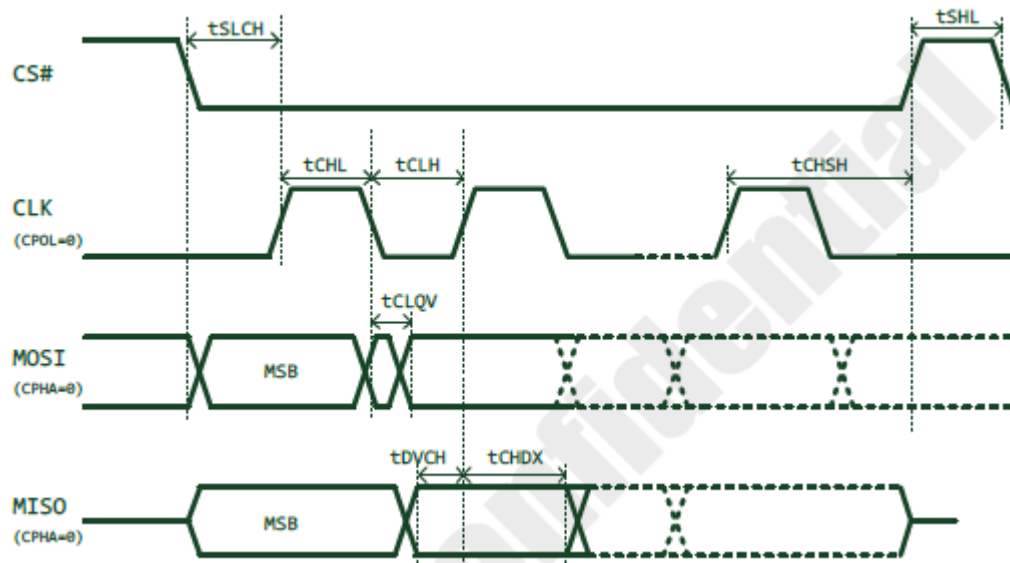


Figure 8: SDIO Timing

Table 3: SDIO Timing Specifications

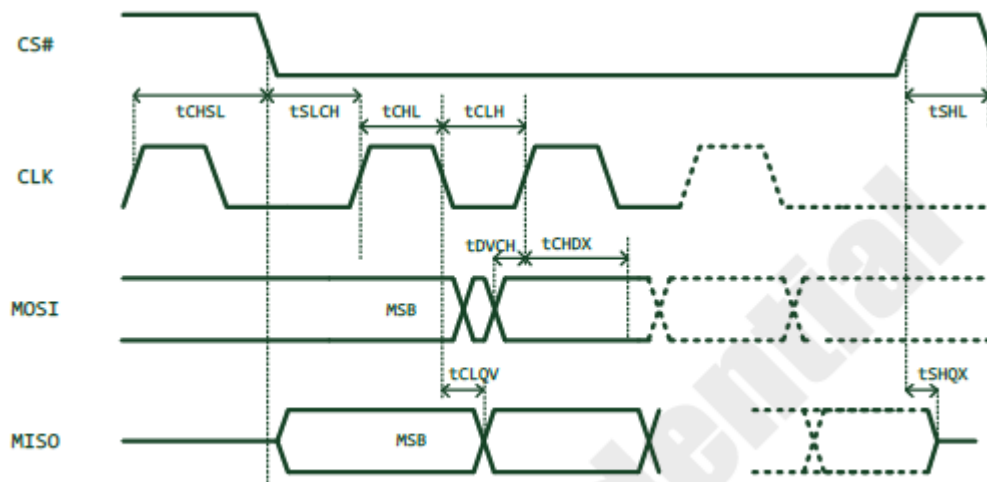
Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SDIO clock frequency	-	(TBD)	-	50	Mhz
SDIO clock high time	tCHL	7	-	-	ns
SDIO clock low time	tCLH	7	-	-	ns
SDIO input setup time	tDVCH	6	-	-	ns
SDIO input hold time	tCHDX	2	-	-	ns
SDIO output delay	Min.: tCHQX, Max.: tCHQV	2.5	-	14	ns

6.4 SPI Master Characteristics



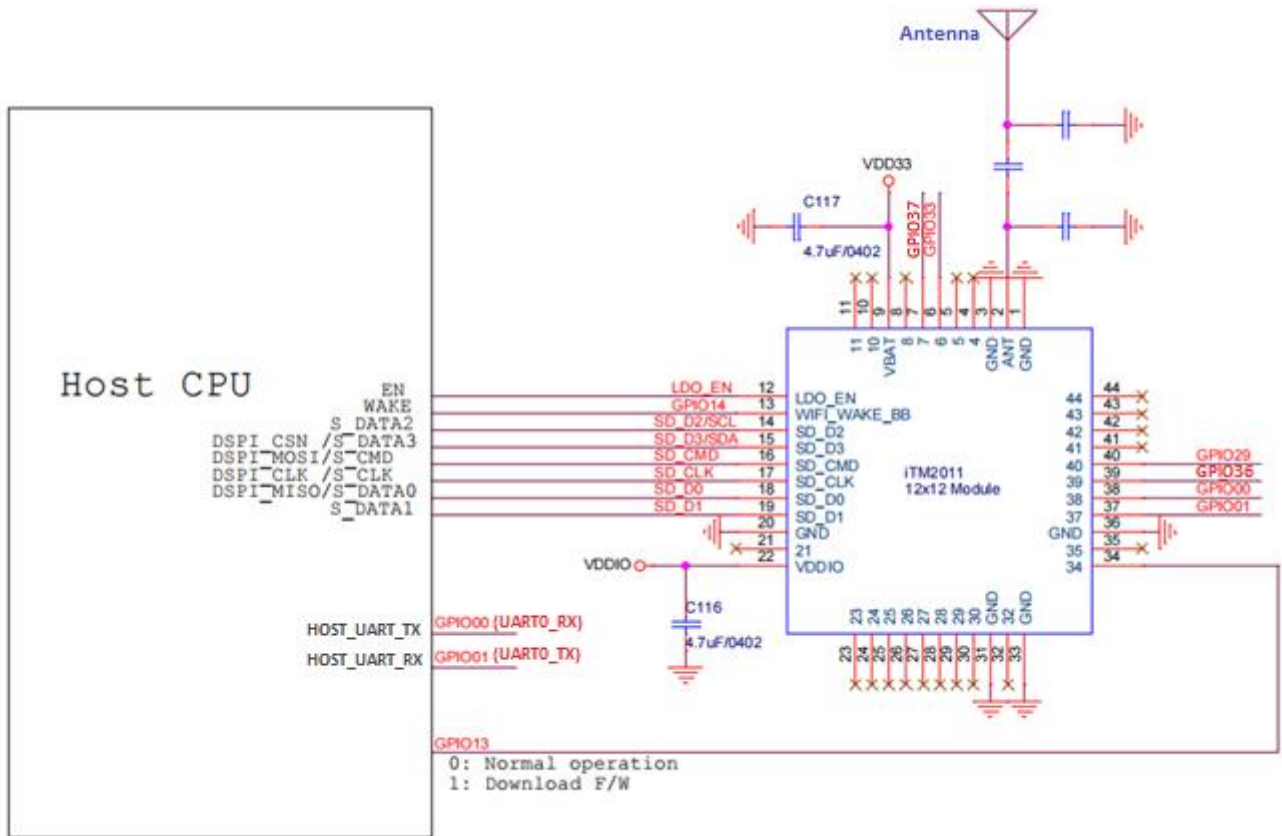
Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SPI Master clock frequency	Clock divided by AHB clock	-	-	20	MHz
SPI Master clock high time	tCHL	22.5	-	-	ns
SPI Master clock low time	tCLH	22.5	-	-	ns
SPI Master CS# hold time	tCHSH	1T CLK	-	-	ns
SPI Master CS# setup time	tSLCH	0.5T CLK	-	-	ns
SPI Master CS# inactive time	tSHL	1T CLK	-	-	ns
SPI Master data in setup time	tDVCH	12	-	-	ns
SPI Master data in hold time	tCHDX	0	-	-	ns
SPI Master data output delay	tCLQV	-	-	2	ns

6.5 Data SPI Slave Characteristics



Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
CS# active hold time	tCHSL	10			ns
CS# active setup time	tSLCH	3			ns
CS# inactive time	tSHL	300			ns
CLK high time	tCHL	12.5			ns
CLK low time	tCLH	12.5			ns
Data in (MISO) setup time	tDVCH	3			ns
Data in (MISO) hold time	tCHDX	3			ns
Data output delay	tCLQV			6.5	ns
Data output disable time	tSHQX			6	ns

7. Reference Design

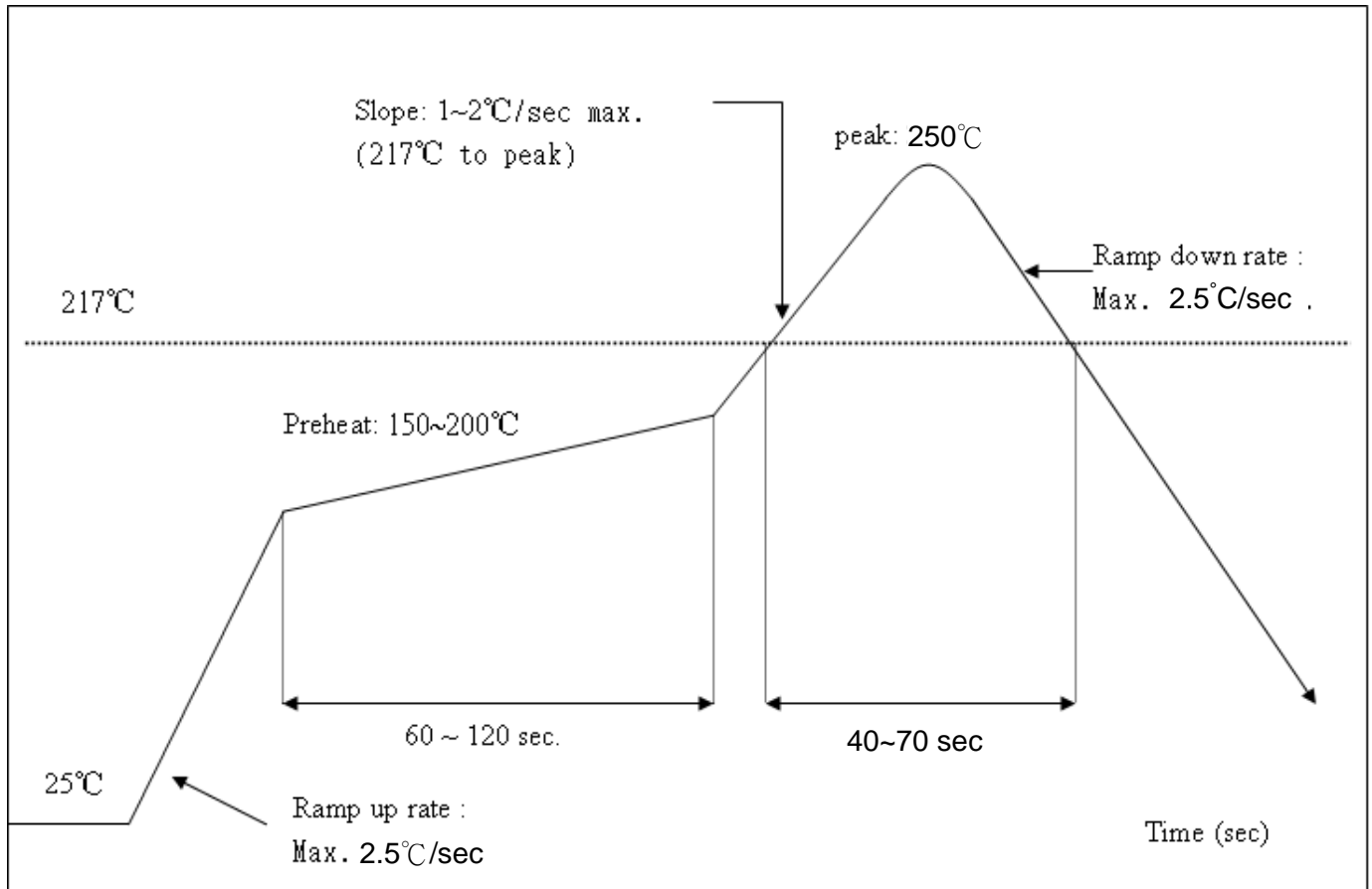


8. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

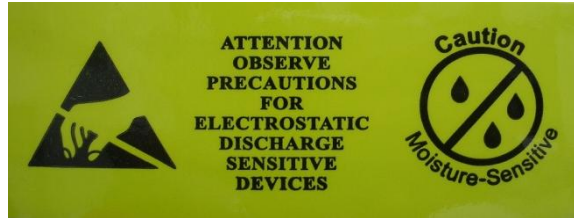
Number of Times : ≤ 2 times



9. Packing Information

9.1 Label

Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition

	Caution	LEVEL <input type="text"/>
	This bag contains MOISTURE-SENSITIVE DEVICES	
<small>If blank, see adjacent bar code label</small>		
1. Calculated shelf life in sealed bag: 12 months at -40°C and <math><90\%</math> relative humidity (RH)		
2. Peak package body temperature: _____ $^{\circ}\text{C}$ <small>If blank, see adjacent bar code label</small>		
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be		
a) Mounted within: _____ hours of factory conditions <small>If blank, see adjacent bar code label</small>		
$\leq 30^{\circ}\text{C}/60\% \text{ RH}$, or		
b) Stored per J-STD-033		
4. Devices require bake, before mounting, if:		
a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$		
b) 3a or 3b are not met		
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure		
Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small>		
<small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small>		

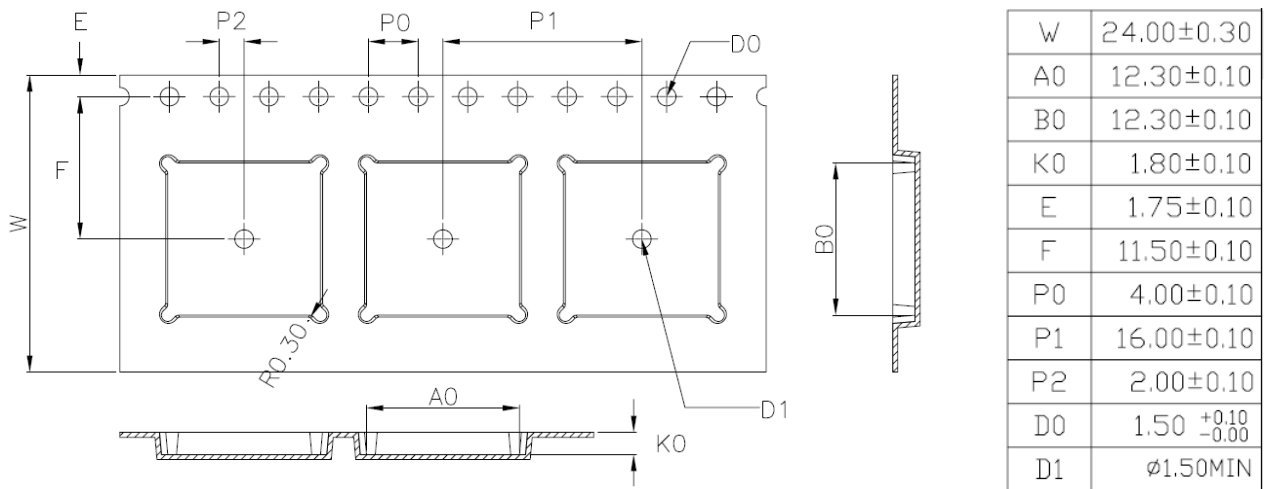
Label C → Inner box label .

PKG S/N :	
	9PKG1201310001
Model:	
	XXXXXXXX(HF)
P/N :	
	99P-W01-0042R
Qty :	
	1500
Date Code :	
	1205
Lot Code :	
	T0C102B

Label D → Carton box label .

iotTech Corporation	
Model Name :	
	XXXXXXXX(HF)
Part No :	
	99P-W01-0042R
Quantity :	
	7500 <small>ea</small>
Lot D/C :	
	1205
Manufacture :	
	2012/02/22

9.2 Dimension



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.

