



iTM1031

IEEE 802.11b/g/n 1T1R WLAN Module Datasheet

Revision History

Date	Revision Content	Revised By	Version
2016/06/17	- Initial released	Ken Wu	1.0
2016/12/20	- Update Description	Issac Chen	1.1
2016/12/20	- Correct Package Information	Ken Wu	1.2

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1. General Description

The iotTech iTM1031 is a low-cost and a highly integrated single-chip WLAN module which has all of the Wi-Fi functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, headsets and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~MCS7, 20MHz, 800ns and 400ns guard interval. The integrated module provides SDIO interface for Wi-Fi.

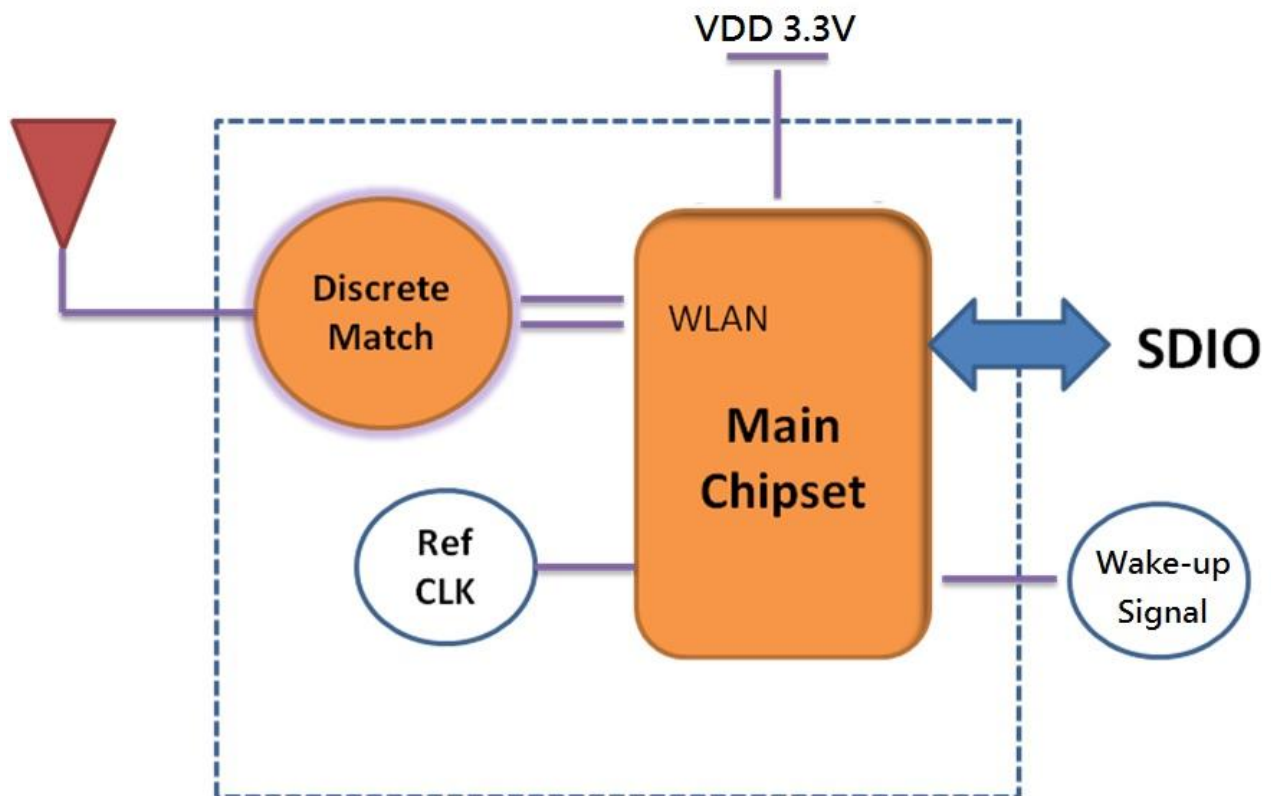
iTM1031 uses iComm SSV6030P Wi-Fi chipset. It has embedded LDOs and DC-DC buck convertor that could provide noise isolation for digital and analog supplies and excellent power efficient with minimum BOM cost.

This compact module iTM1031 is a total solution for Wi-Fi technologies. It is specifically developed for portable devices, and can minimize the resource consumption of CPU and memory for enabling Wi-Fi communication.

2. Features

- Wi-Fi Chipset : iComm SV6030P
- Integrated WLAN CMOS efficient power amplifier with internal power detector and closed loop power calibration
- Single stream 802.11n provides highest throughput and superior RF performance for handhelds.
- Advanced 1X1 802.11n features:
 - Full / Half Guard Interval
 - Frame Aggregation
 - Reduced Inter-frame Space (RIFS)
 - Space Time Block Coding (STBC)
 - Greenfield mode
- Supports popular interfaces: SDIO 2.0 (50MHz, 4-bit and 1-bit) and SPI_SLAVE mode
- Integrated MCU with on-chip memory to share the loading of host CPU for Wi-Fi communication

The block diagram of iTM1031 module is depicted in the figure below.



3. General Specification

3.1 Voltages

3.1.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.3	3.6	V

3.1.2 Recommended Operating Ratings

Test conditions: At room temperature				
Symbol	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.6	V

Note: The I/O voltage of ITM1031 same as VBAT.

Test conditions: At operating temperature -10°C ~70°C				
Symbol	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.6	V

3.2 Wi-Fi RF Specification (RX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2412		2484	MHz
RX Sensitivity 11b @ 8% PER	- 1Mbps		-91		dBm
	- 2Mbps		-89		dBm
	- 5.5Mbps		-87		dBm
	- 11Mbps		-85		dBm
RX Sensitivity 11g @ 10% PER	- 6Mbps		-89		dBm
	- 9Mbps		-88		dBm
	- 12Mbps		-84		dBm
	- 18Mbps		-82		dBm
	- 24Mbps		-79		dBm
	- 36Mbps		-76		dBm
	- 48Mbps		-73		dBm
	- 54Mbps		-71		dBm
Receive Sensitivity (11n,20MHz) @10% PER	- MCS0		-87		dBm
	- MCS=1		-84		dBm
	- MCS=2		-82		dBm
	- MCS=3		-78		dBm
	- MCS=4		-75		dBm
	- MCS=5		-71		dBm
	- MCS=6		-70		dBm
	- MCS=7		-69		dBm
Maximum Receive Level	802.11b		-10		dBm
	802.11g		-8		dBm
	802.11n		-8		dBm
Operating temperature	-10°C to 70°C				
Storage temperature	-40°C to 85°C				

3.3 Wi-Fi RF Specification (TX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2412		2484	MHz
Output Power	802.11b		17		dBm
	802.11g		15		dBm
	802.11n		14		dBm
@EVM	802.11b		-19		dB
	802.11g		-28		dB
	802.11n		-30		dB
Harmonic Level @ Ant Port (17dBm with 100% duty cycle, CCK, 1Mbps)	4.8-5GHz, 2 nd harmonic		-56		dBm/ 1MHz
	7.2-7.5GHz, 3 rd harmonic		-80		dBm/ 1MHz

3.4 Power Consumption

(DC-DC mode, DC-DC bulk-converter enabled)

WLAN Operational Modes	Typ.	Unit
OFF ^a	4	uA
Rx, CCK, 1 Mbps	60	mA
Rx, OFDM, 54 Mbps	66	mA
Rx, HT20, MCS7	67	mA
Sleep	200	uA
Rx Power Saving, DTIM= 1	1.2	mA
Tx, CCK, 1 Mbps, 19dBm	282	mA
Tx, OFDM, 54 Mbps, 16dBm	218	mA
Tx, HT20, MCS7, 15dBm	223	mA

a. Test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V

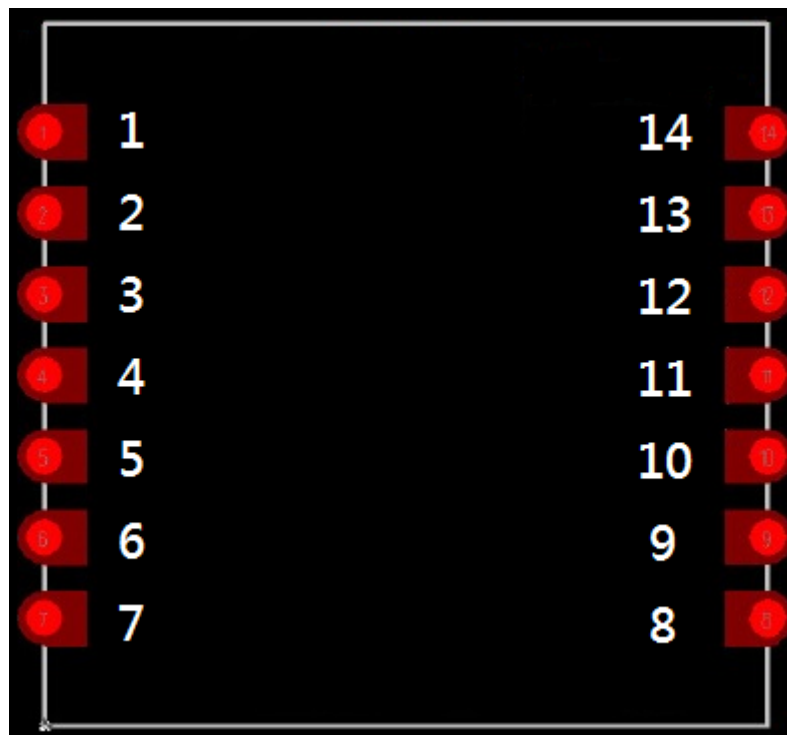
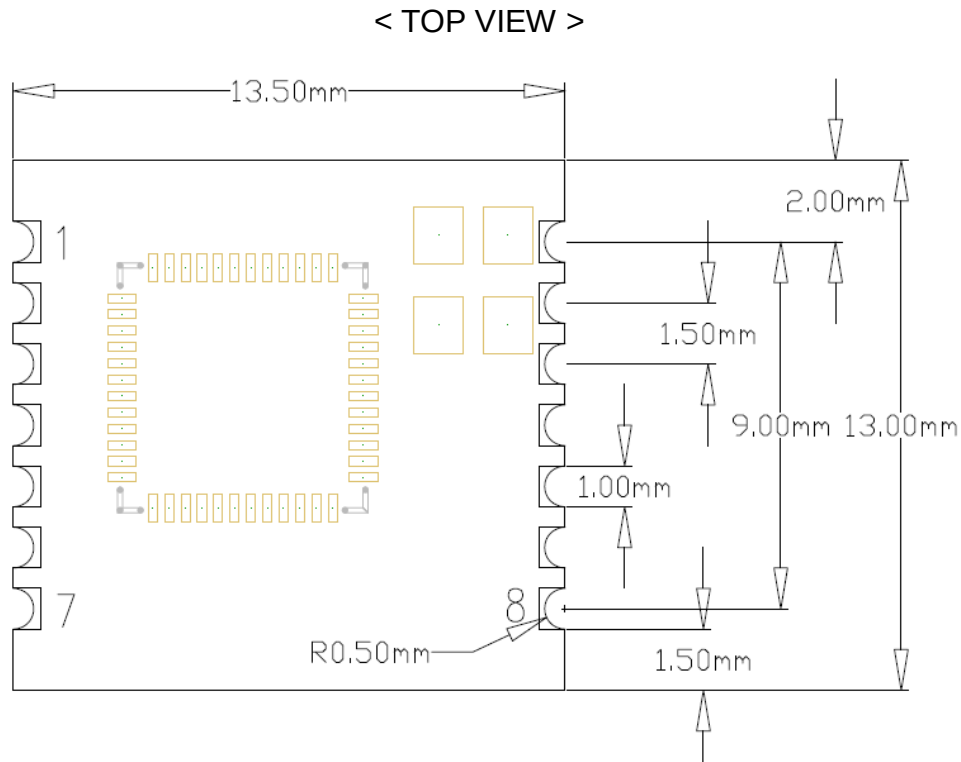
(LDO mode, DC-DC bulk-converter disabled)

WLAN Operational Modes	Typ.	Unit
OFF ^b	4	uA
Rx, CCK, 1 Mbps	91	mA
Rx, OFDM, 54 Mbps	101	mA
Rx, HT20, MCS7	103	mA
Tx, CCK, 1 Mbps	290	mA
Tx, OFDM, 54 Mbps	237	mA
Tx, HT20, MCS7	239	mA

b. Test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V

4. Pin Assignments

4.1 PCB Pin Outline



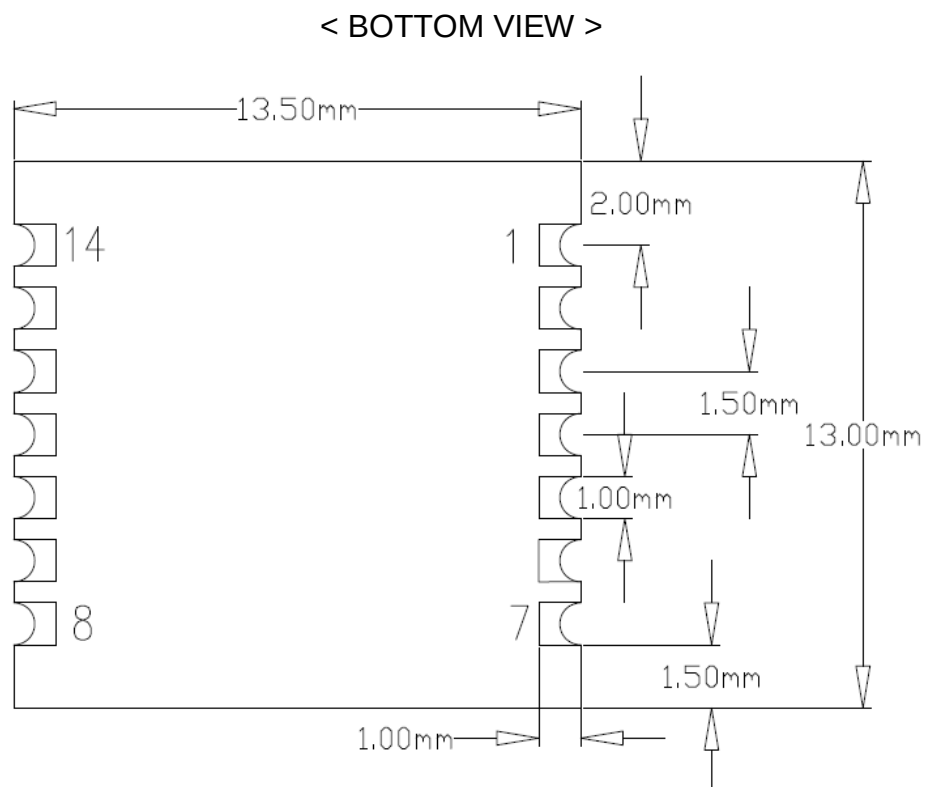
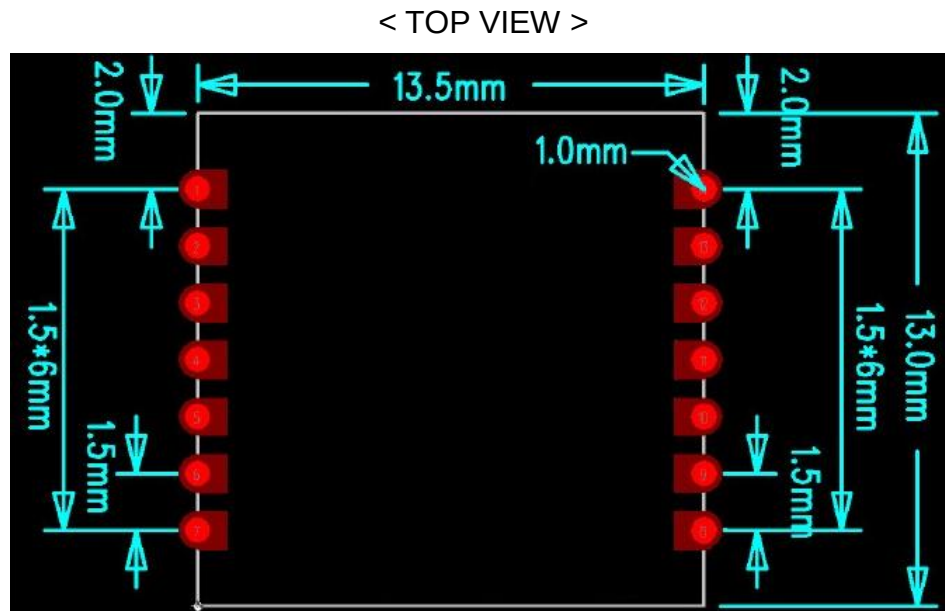
4.2 Pin Definition

NO	Name	Type	Description
1	SDIO_DATA_2	I/O	SDIO data line 2
2	SDIO_DATA_3	I/O	SDIO data line3
3	SDIO_DATA_CMD	I/O	SDIO command line
4	GND	—	Ground connections
5	SDIO_DATA_CLK	I/O	SDIO CLK line
6	SDIO_DATA_0	I/O	SDIO data line 0
7	SDIO_DATA_1	I/O	SDIO data line 1
8	VBAT	P	Main power voltage source input
9	LDO_EN	I	WLAN device power enable/disable
10	GND	—	Ground connections
11	RF_OUT	I/O	RF I/O port
12	GND	—	Ground connections
13	NC	—	Floating (Don't connect)
14	WL_HOST_WAKE	O	WLAN wake-up HOST Pin14 MUST be floating or connected to an input pin of host CPU and DO NOT drive pin14 to low voltage

5. Dimensions

5.1 Layout Recommendation

(Unit: mm)



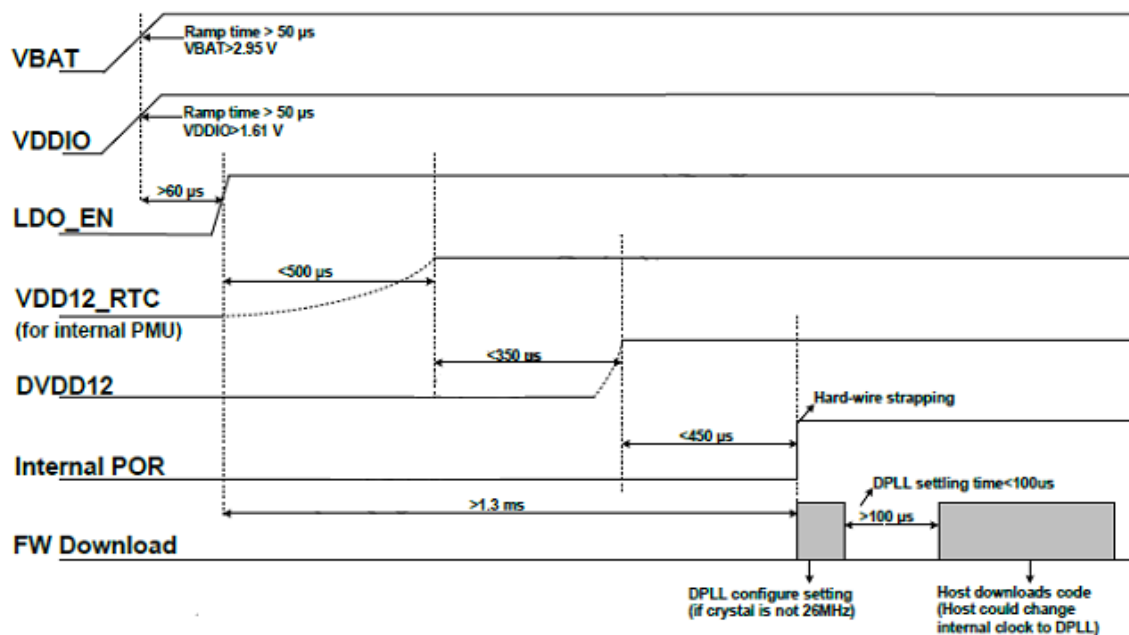
6. Host Interface Timing Diagram

6.1 Power UP Sequence

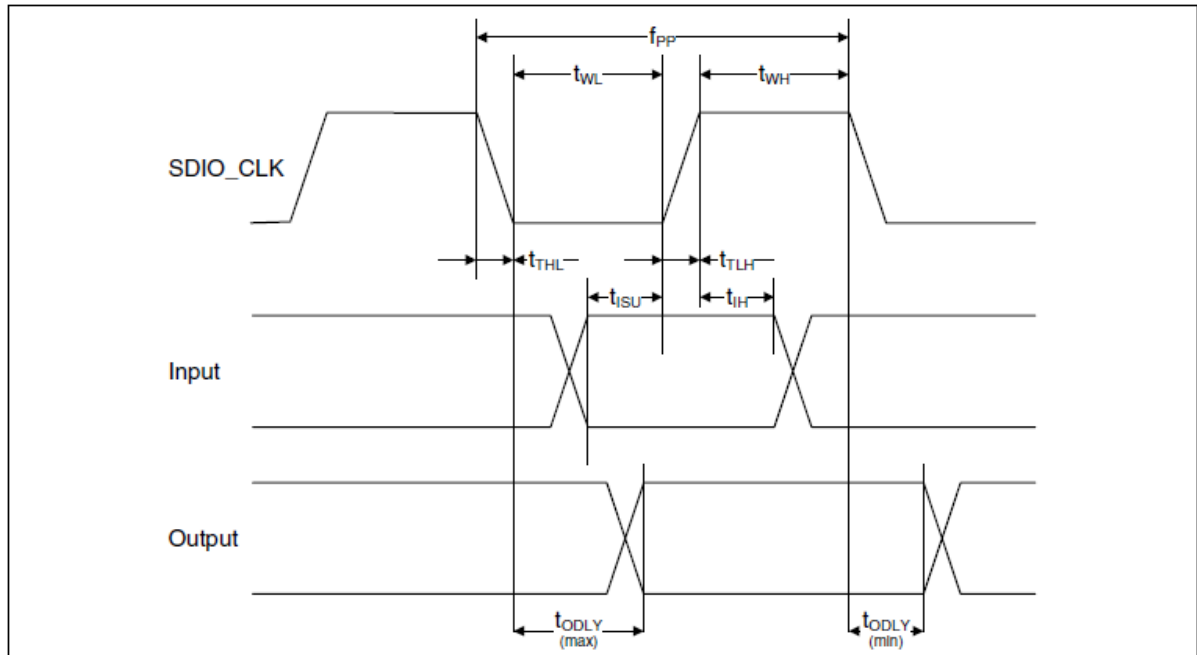
Shows the below figure, the power-on sequence of the iTM1031 from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. After initial power-on, the LDO_EN signal can be held low to turn off the iTM1031.

After LDO_EN is assert and host starts the power-on sequence of the iTM1031. From that point, the typical power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.



6.2 SDIO Default Mode Timing Diagram

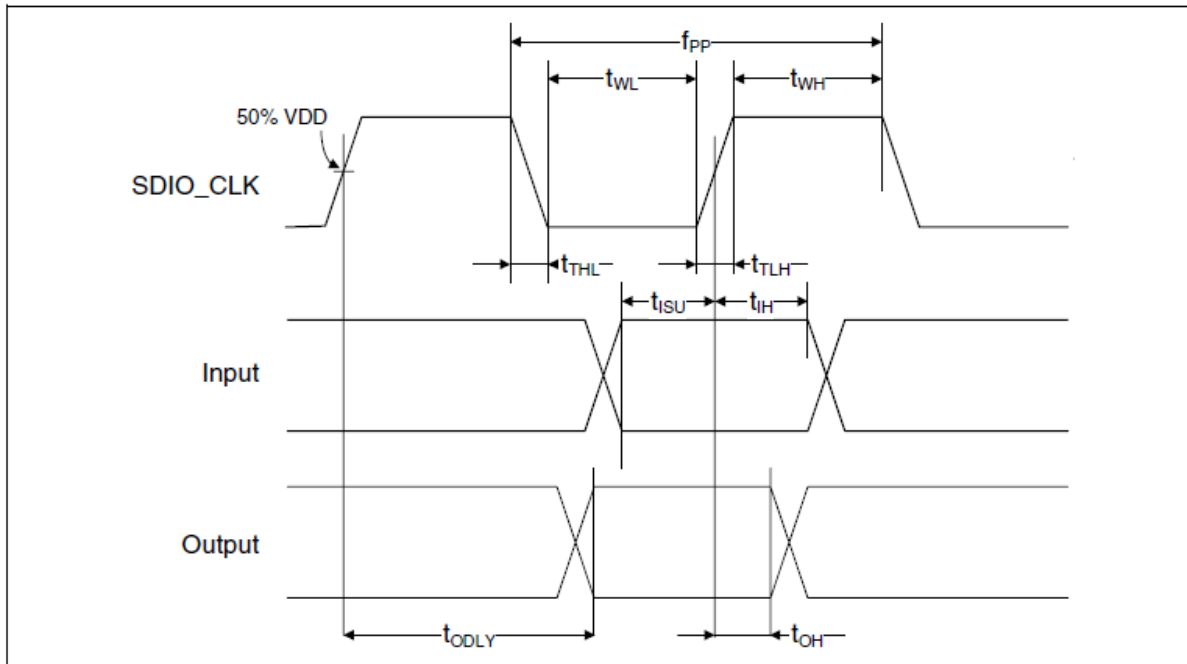


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency-Data Transfer mode	f_{PP}	0	-	25	MHz
Frequency-Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	10	-	-	ns
Clock high time	t_{WH}	10	-	-	ns
Clock rise time	t_{TLH}	-	-	10	ns
Clock low time	t_{THL}	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	-	-	ns
Input hold time	t_{IH}	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	0	-	14	ns
Output delay time - Identification mode	t_{ODLY}	0	-	50	ns

a. Timing is based on $C_L \leq 40\text{pF}$ load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

6.3 SDIO High Speed Mode Timing Diagram

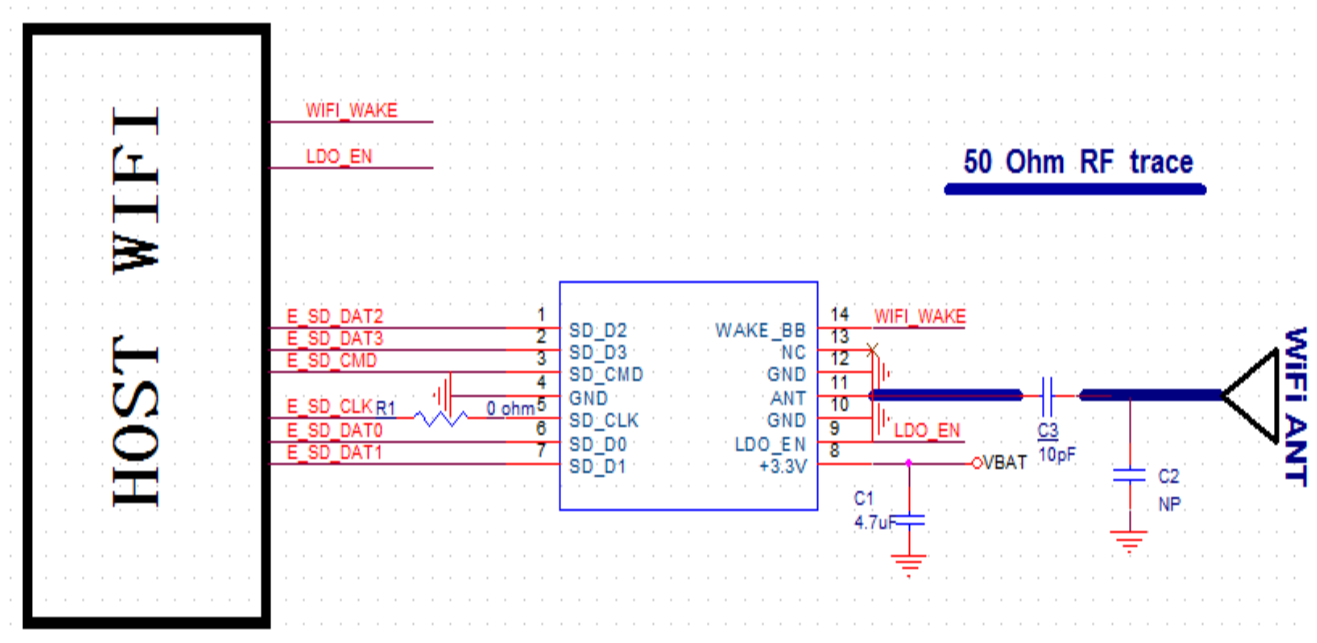


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency-Data Transfer mode	f_{PP}	0	-	50	MHz
Frequency-Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	7	-	-	ns
Clock high time	t_{WH}	7	-	-	ns
Clock rise time	t_{TLH}	-	-	3	ns
Clock low time	t_{THL}	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6	-	-	ns
Input hold time	t_{IH}	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	-	-	14	ns
Output hold time	t_{OH}	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on $CL \leq 40\text{pF}$ load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

7. Reference Design



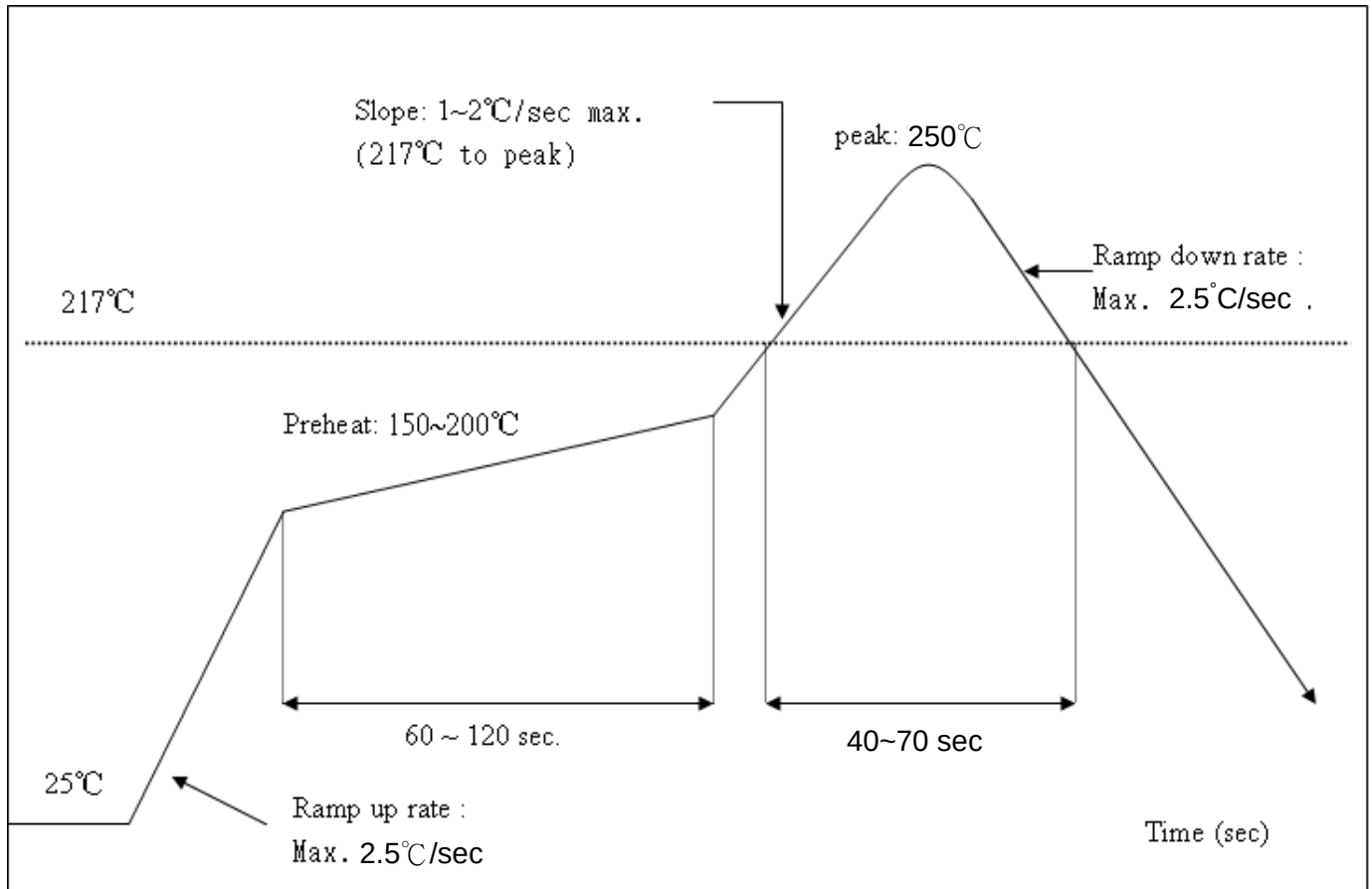
- The cascaded resistor R1 in the trace of SDIO clock **MUST** be reserved, and the value of R1 depends on the host controller and PCB.

8. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : $<250^{\circ}\text{C}$

Number of Times : ≤ 2 times



9. Packing Information

9.1 Label

Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition

	Caution	LEVEL
	This bag contains MOISTURE-SENSITIVE DEVICES	 If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label ≤30°C/60% RH, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

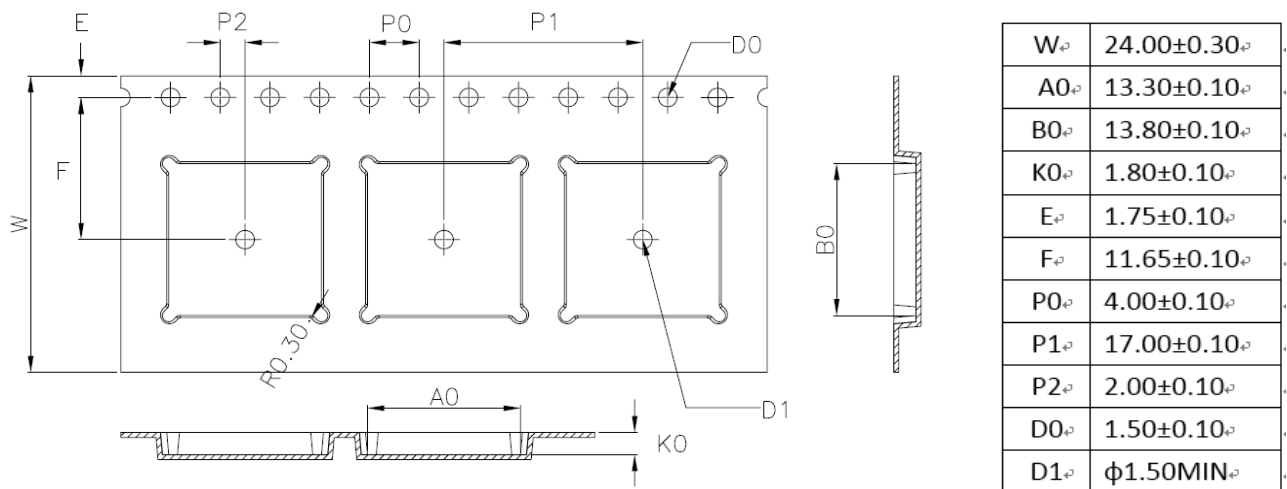
Label C → Inner box label .

PKG S/N :	
Model:	
P/N :	
Qty :	
Date Code :	
Lot Code :	

Label D → Carton box label .

iotTech Corporation	
Model Name :	
Part No :	
Quantity :	
Lot D/C :	
Manufacture :	

9.2 Dimension



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.

